

**Birla Vishvakarma Mahavidyalaya**

**Engineering Collage (An Autonomous Institution)**

**Vallabh Vidyanagar - 388 120**

**Affiliated to Gujarat Technological University**

**A.Y. 2023**

# Assignment : II

**Course Title:** Digital System Design

**Name:** Akshay Singh

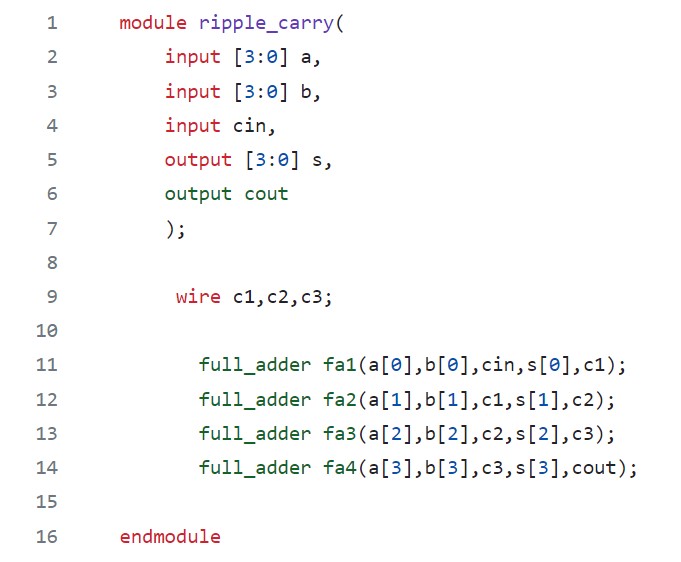
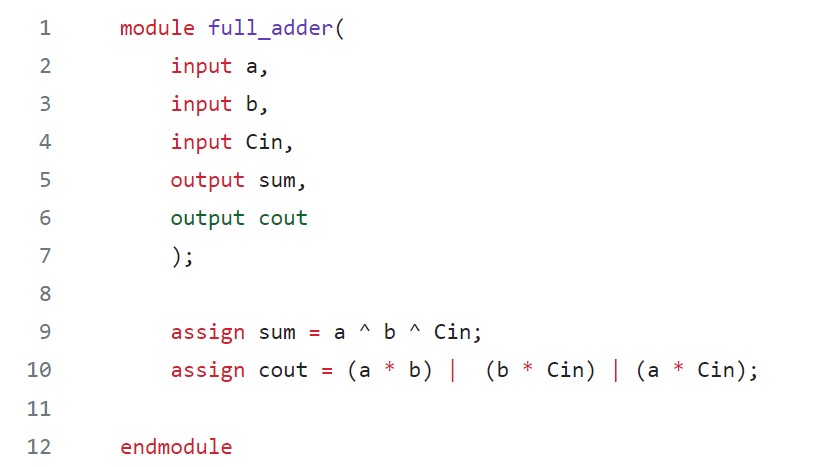
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**Batch:** A11

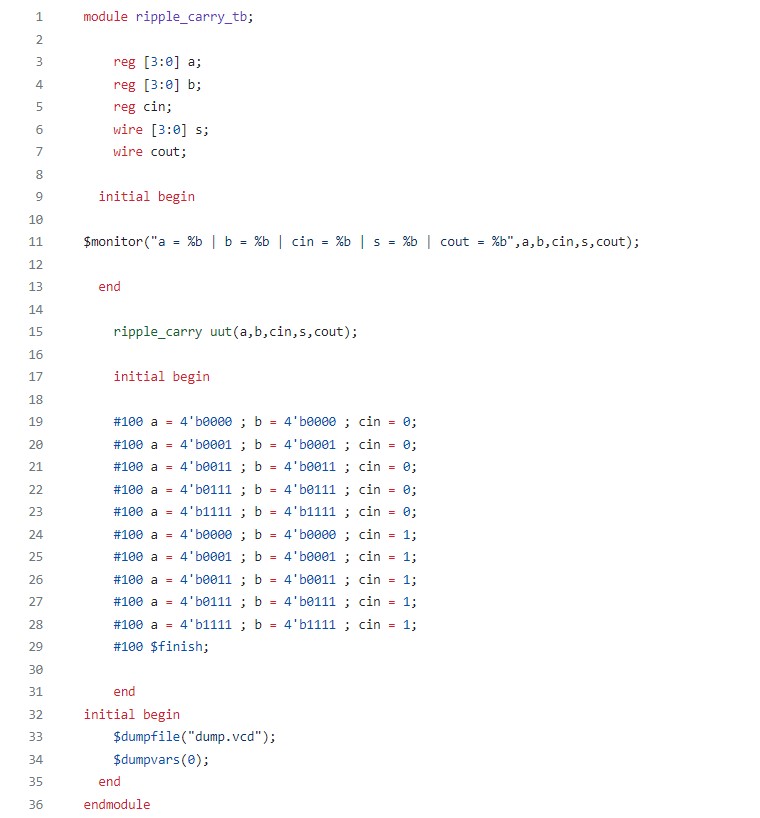
**Course Code:** 3EL42

**Q.1) Design 4-bit Ripple Carry Adder with the help of 1-bit adder.**

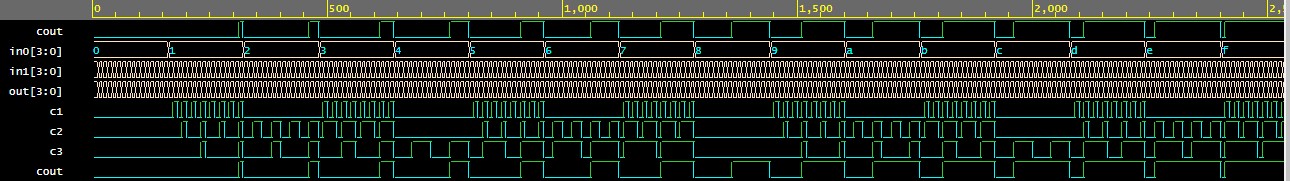
**CODE:**



**TESTBENCH:**

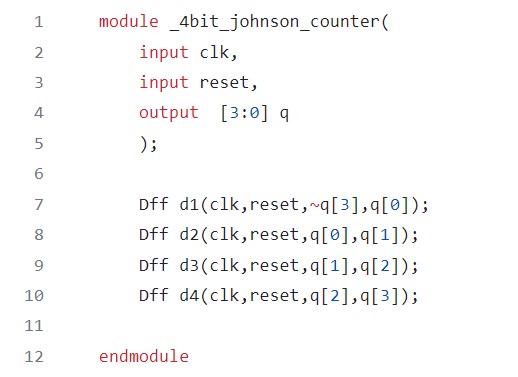
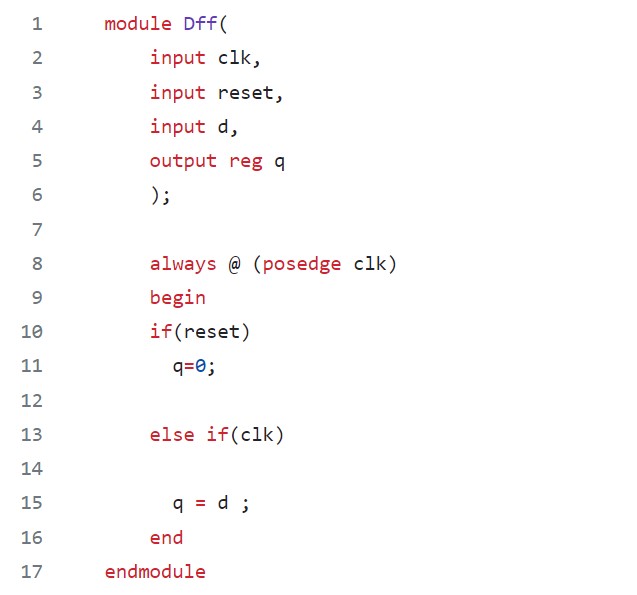


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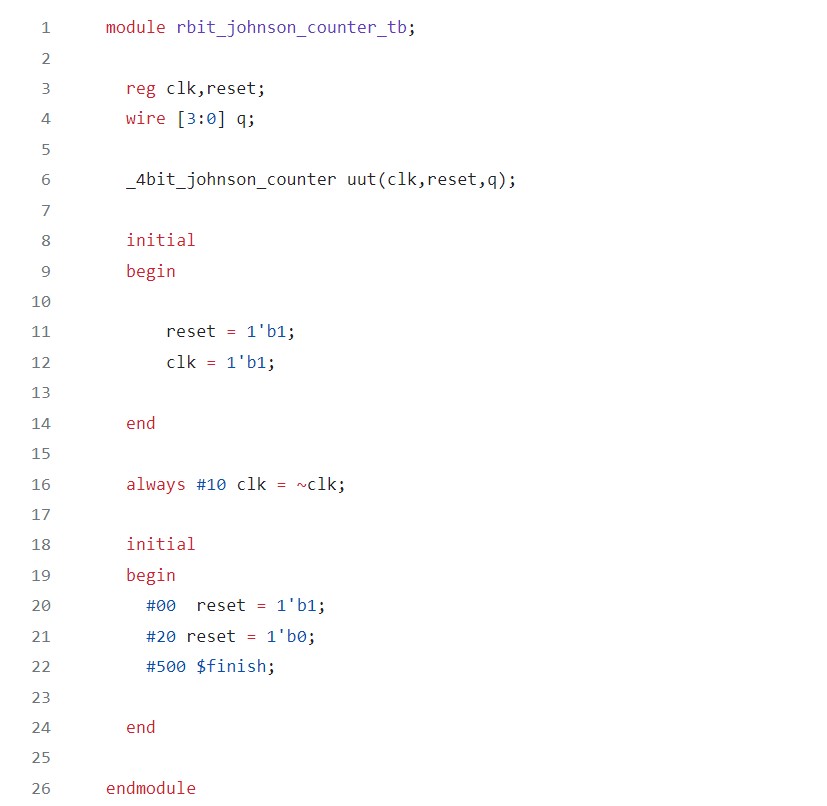


**Q.2) Design a D-flip flopand reuse it to implement 4-bit Johnson Counter.**

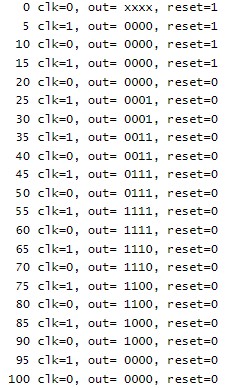
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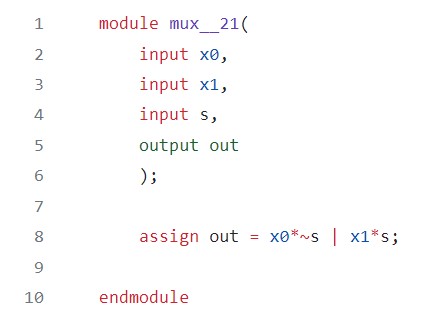


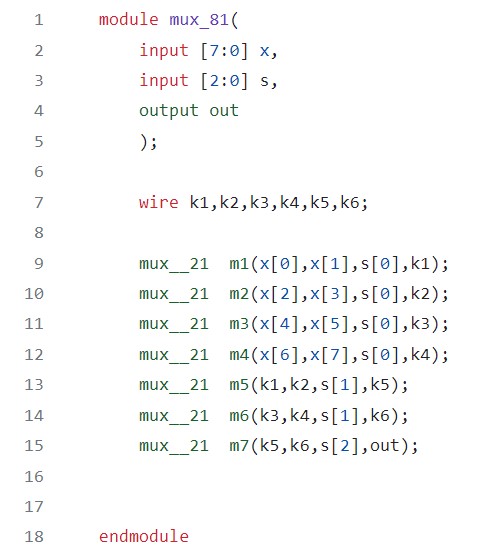
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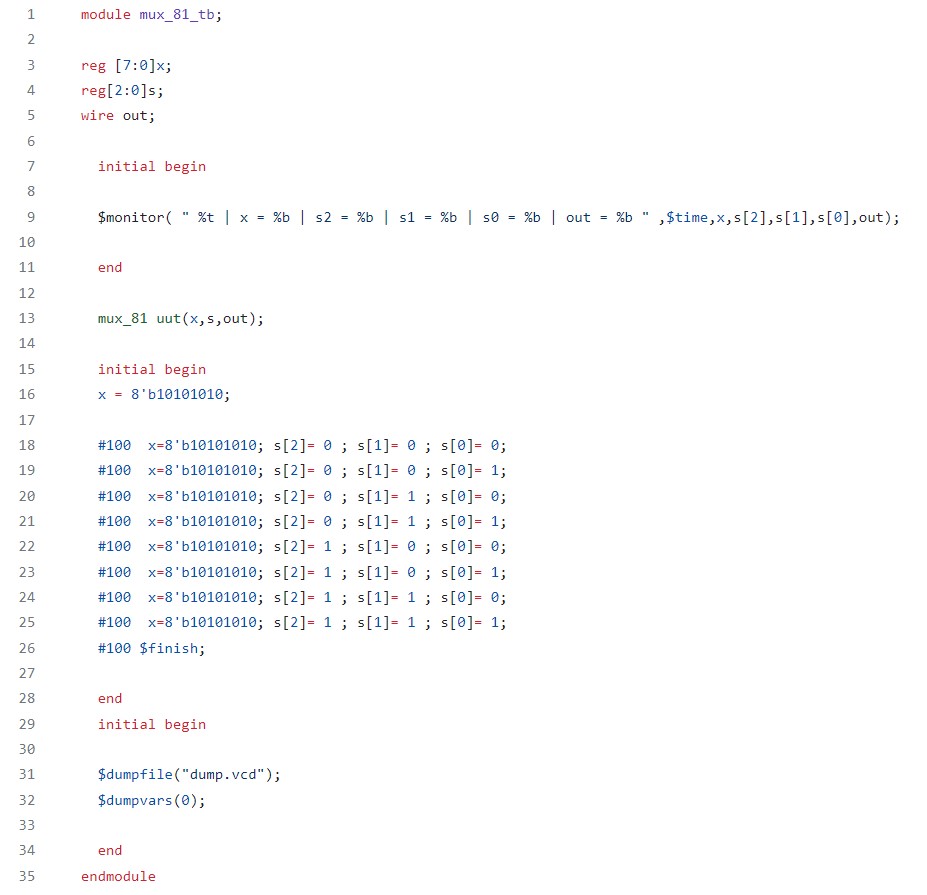
**Q.3) Reuse 2:1 Mux code to implement 8:1 Mux.**

**CODE:**

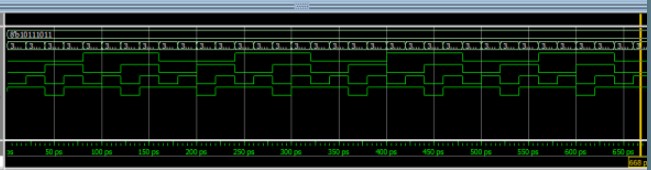




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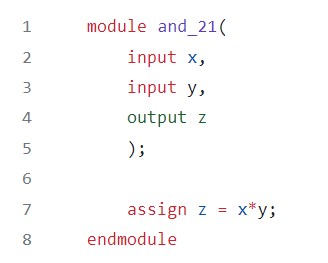


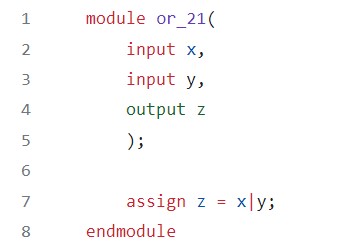
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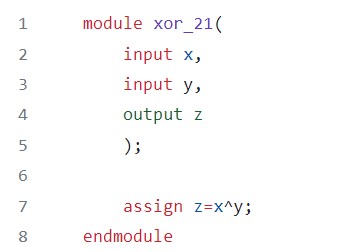


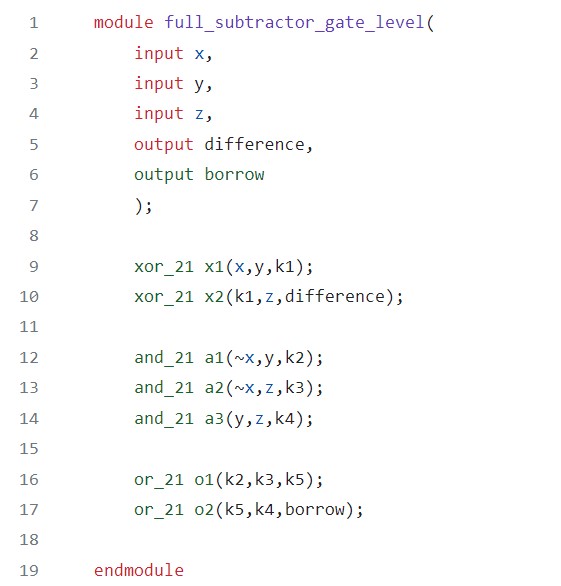
**Q.4) Design a Full Substractor with Gate Level Modelling style.**

**CODE:**

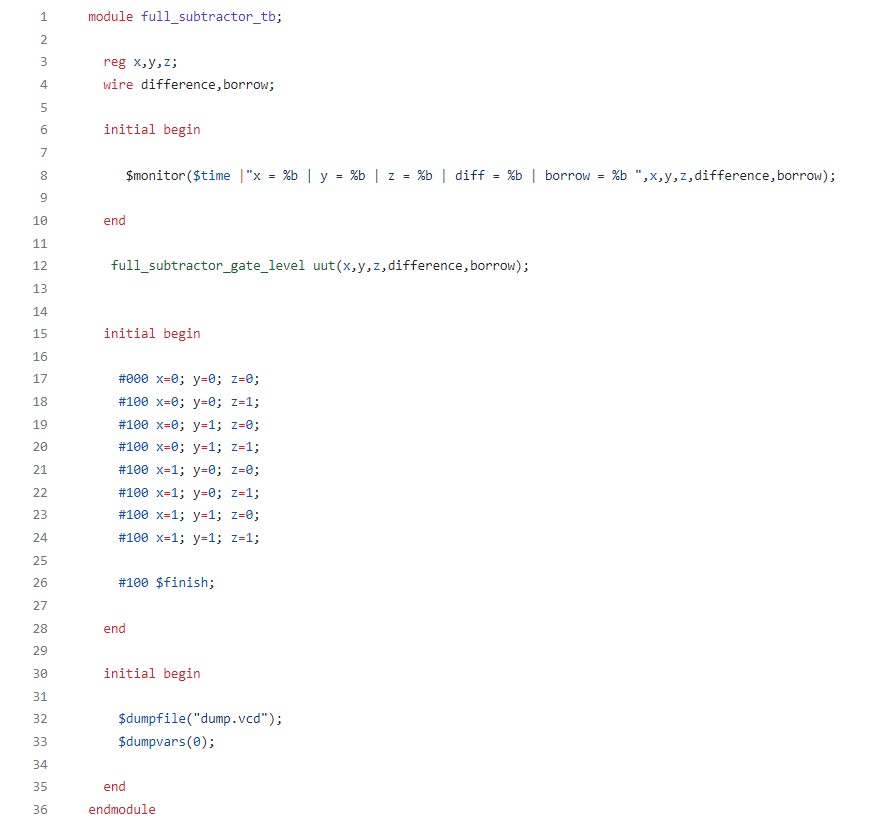




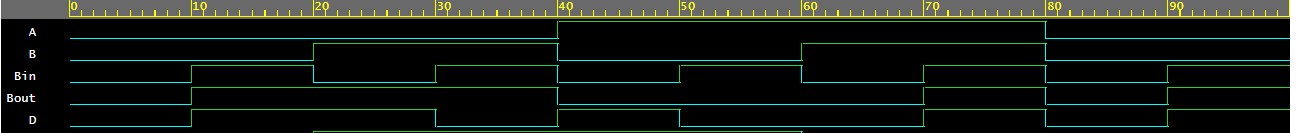




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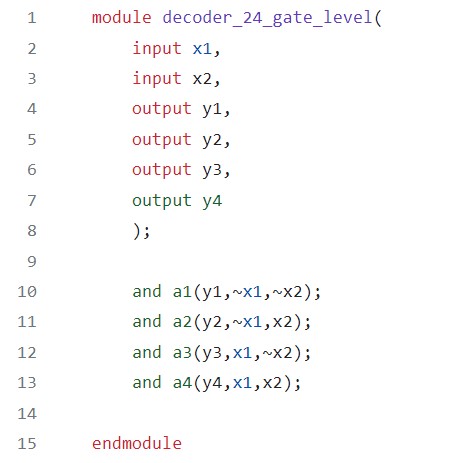


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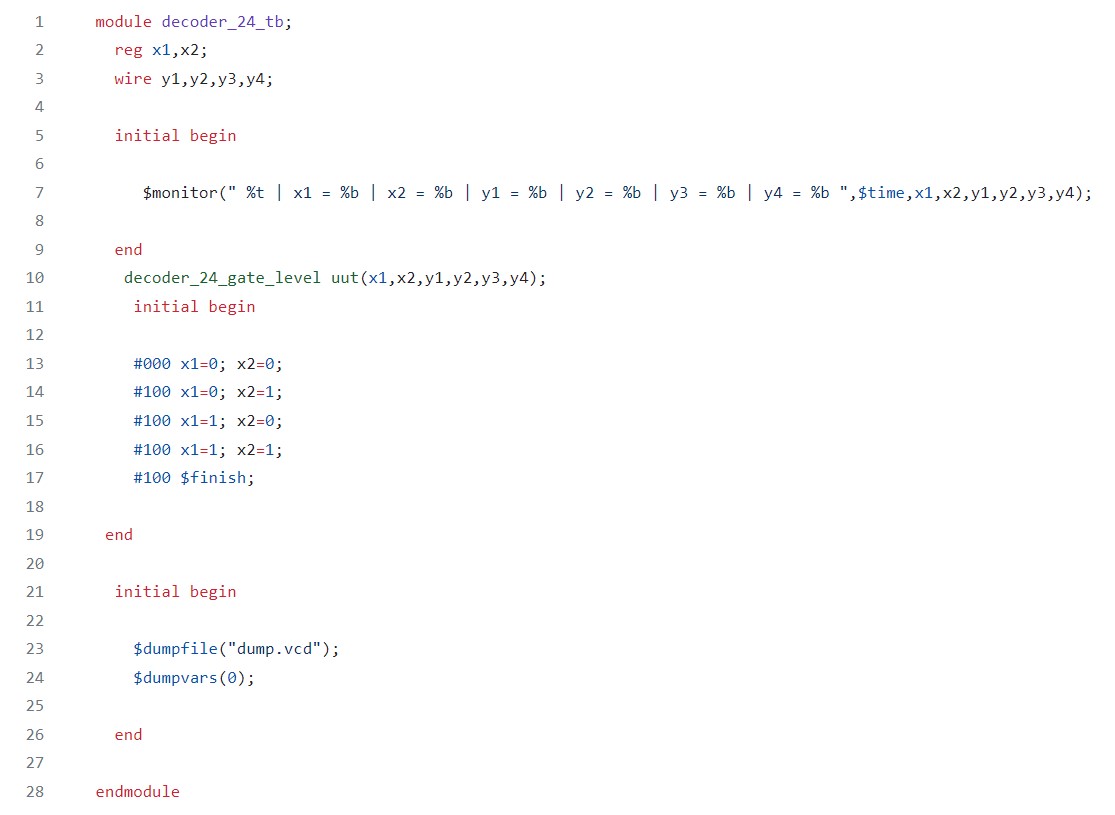


**Q.5) Design a 2 x 4 Decoder using gate level modelling.**

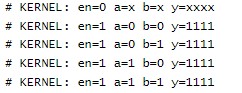
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**TESTBENCH:**

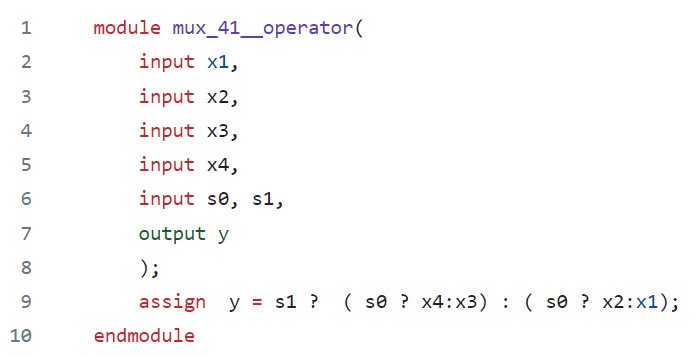


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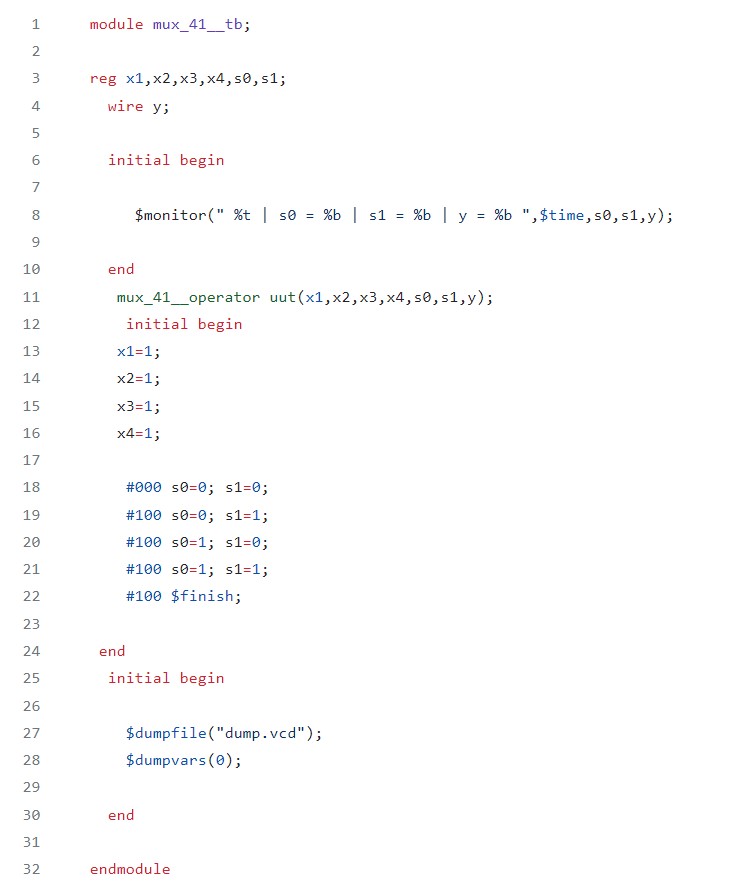


**Q.6) Design a 4x1 Mux using operators (use data flow).**

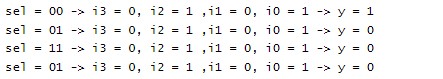
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**TESTBENCH:**

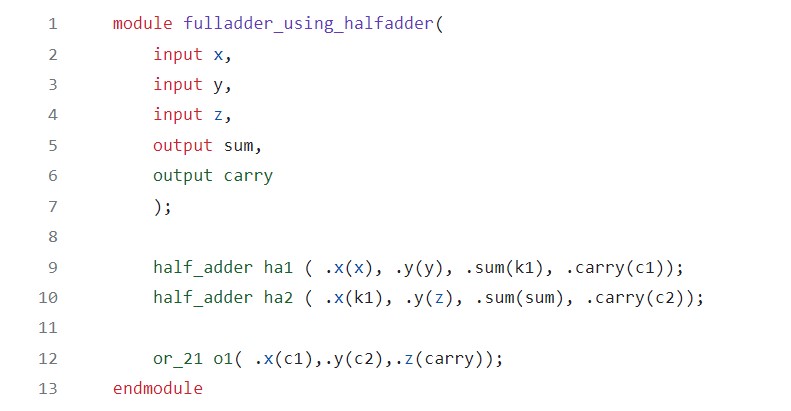
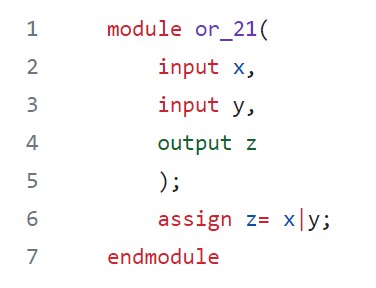
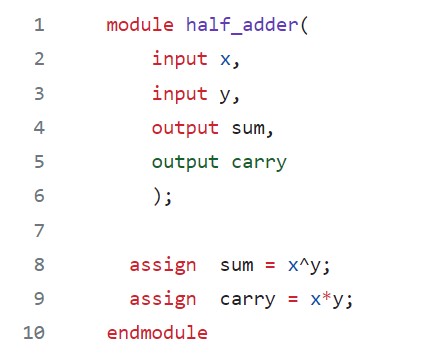


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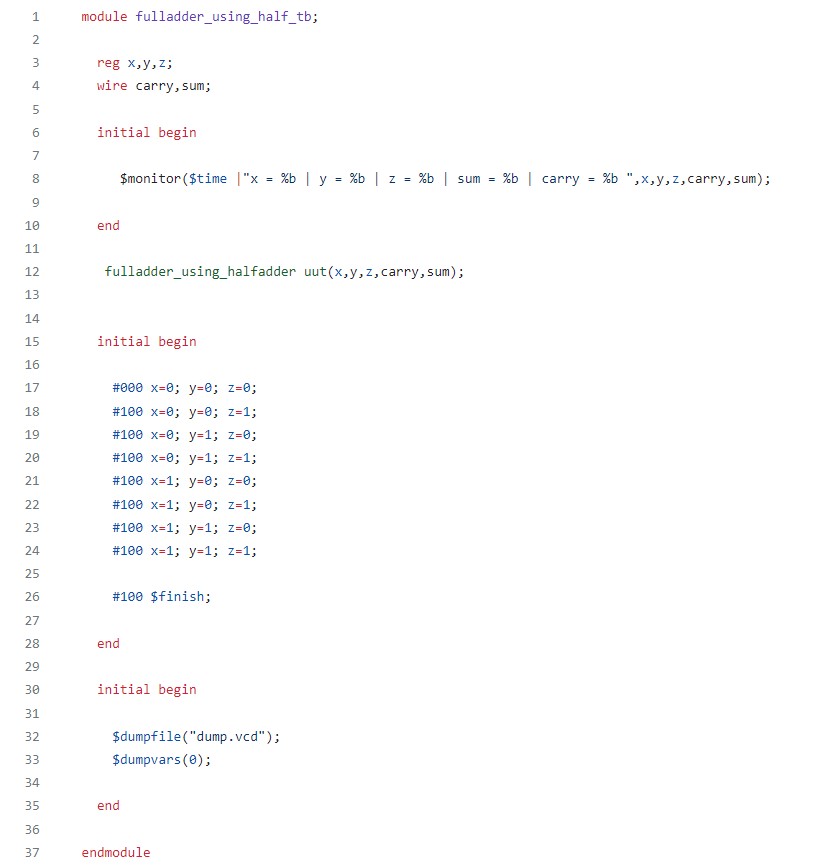


**Q.7) Design a Full adder using half adder.**

**CODE:**



**TESTBENCH:**



**OUTPUT:**

